



S/N 09/945,507

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al. Examiner: Son T. Dinh
Serial No.: 09/945,507 Group Art Unit: 2824
Filed: August 30, 2001 Docket: 1303.014US1
Title: FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY
INSULATORS

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date/Issue Date</u>	<u>Attorney Docket</u>	<u>Title</u>
11/062543	February 22, 2005	1303.028US2	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
11/063825	February 23, 2005	1303.132US1	GERMANIUM-SILICON-CARBIDE FLOATING GATES IN MEMORIES
11/063717	February 23, 2005	1303.134US1	ATOMIC LAYER DEPOSITION OF Hf3N4/HfO2 FILMS AS GATE DIELECTRICS
11/168004	June 28, 2005	1303.043US3	ASYMMETRIC BAND-GAP ENGINEERED NONVOLATILE MEMORY DEVICE
11/202460	August 12, 2005	1303.027US3	SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
11/189075	July 25, 2005	1303.148US1	MAGNESIUM TITANIUM OXIDE FILMS

Continuations and divisionals may be later filed on the cases listed above, or cited to the Examiner in any previous Communication Concerning Related Applications. Applicants request that the Examiner review all continuations and divisionals of the above-listed or previously-cited patent applications before allowing the claims of the present patent application.

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Respectfully submitted,

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By



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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 2 day of September, 2005.

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